HIGH EFFICIENCY MODE CHARACTERIZATION IN A 20 GHz MBE GaAs IMPATT DIODE AMPLIFIER

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ABSTRACT

A high efficiency mode in a 20 GHz MBE-grown single drift GaAs Read-type IMPATT diode has been observed by using a computer-aided characterization system. The intrinsic diode is estimated to have 2 W power capability with 26% efficiency at 22 GHz. The diode was tested in a modified top-hat amplifier circuit to demonstrate 3.1 GHz bandwidth at 3.7 dB gain with 3 W maximum output power.

Introduction

There has been a great need for high power, high efficiency solid state devices for various types of applications at microwave frequencies and above. IMPATT diodes have been one of the best contenders to meet this requirement. Since the experimental achievement of high efficiency in GaAs Read-type IMPATT diodes[1], great efforts have been made to increase their power capability and operating frequency.

This paper describes the experimenal observation of a high efficiency mode in a 20 GHz GaAs Read-type IMPATT diode. The first section gives a brief description of a computer-aided characterization system used in this work. The diode has been embedded in an amplifier circuit, newly developed for wideband operation, to provide the overall performance presented in the last section.

Computer-aided characterization system

A new system has been developed for fast and accurate characterization of IMPATT amplifiers. A PDP-11 computer is directly linked to the system for real-time data collection and processing so that the results can be displayed immediately either on a CRT, an X-Y recorder, or on a console typewriter.

The system not only measures the admittance of an IMPATT diode but also characterizes an amplifier circuit in terms of circuit admittance and circuit efficiency. The junction temperature of the diode is monitored continuously during measurement on a digital meter, provided that its thermal resistance is known.

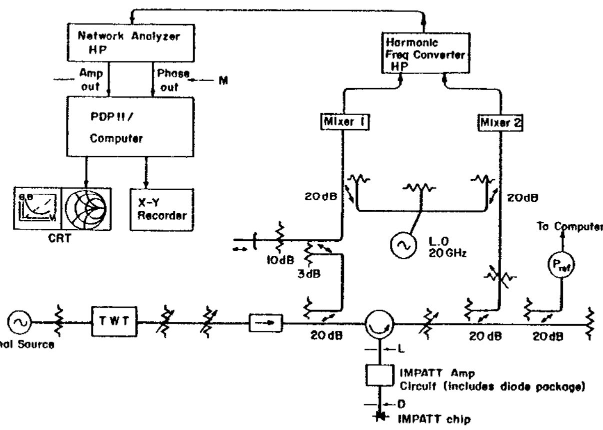

Fig. 1 Schematic diagram of a computer-aided characterization system.

Fig. 1 is a schematic diagram of the system for 20 GHz and higher frequencies. It is basically a network analyzer with a down converter section. The input power is delivered through a circulator to a stabilized IMPATT amplifier at the test port. The admittance of the IMPATT diode is measured after two matrices are determined, each of which represents the network analyzer and the amplifier circuit respectively. The amplifier circuit is characterized by using the junction capacitance of the diode as a reference admittance so that the series resistance of the diode is measured in this step. Least square techniques have been used to minimize possible random errors. The accuracy of measurement has been estimated to be less than 15%. The time required for diode characterization at a given frequency is less than 15 minutes, including time for calibration.

Fig. 2 is shown to demonstrate the sensitivity of the system. The measured series resistance of a GaAs Hi-Lo IMPATT diode is plotted as a function of distance or depletion width. The change of slope at 0.3 μm clearly shows the edge of the avalanche zone.

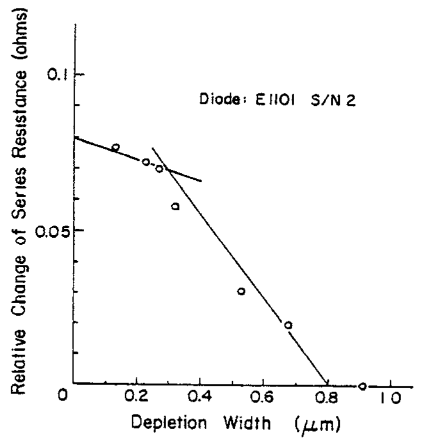

Fig. 2 Relative change of a series resistance measured at 20 GHz as a function of a depletion width.

Observation of high efficiency mode

A high efficiency mode has been observed by this computer-aided characterization system in a 20 GHz Varian MBE-grown GaAs IMPATT diode. The diode is a single mesa P+ Hi-Lo structure with doping concentrations $N_H = 1.5 \times 10^{17}$ cm^{-3} and $N_L = 1.0 \times 10^{16}$ cm^{-3}. The total active layer is 2.3 μm in length with a 0.3 μm well-defined avalanche zone and the diode area is

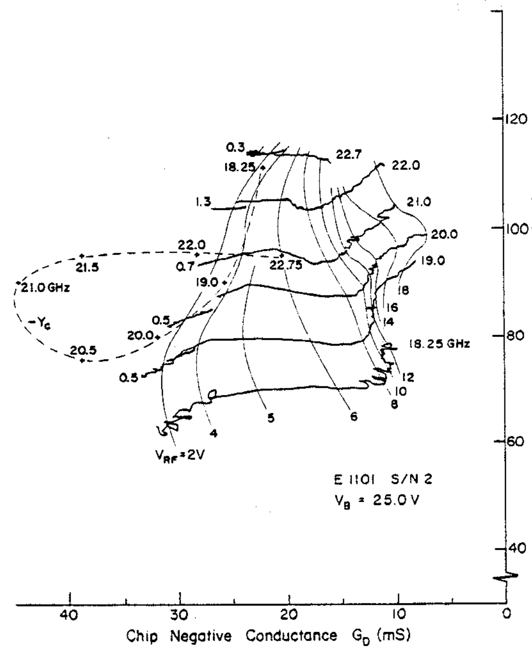

Fig. 3 Measured chip admittance of a MBE-grown GaAs IMPATT diode. Bias voltage = 25.0 V.

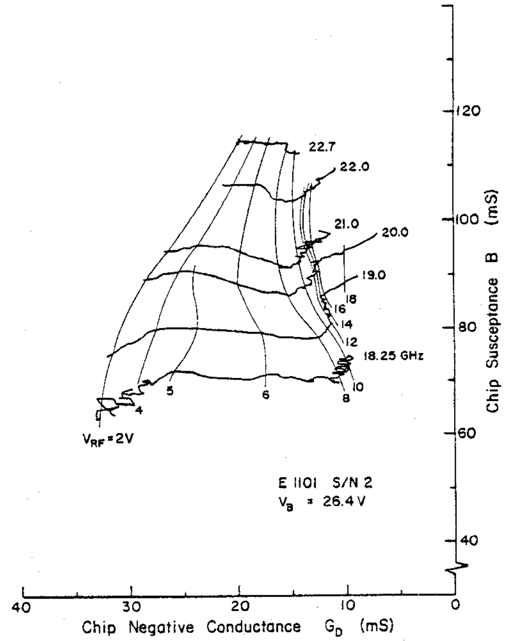

Fig. 4 Measured chip admittance of a MBE-grown GaAs IMPATT diode. Bias voltage = 26.4 V.

1.1×10^{-4} cm^2. At the typical operating point of 26 V and 260 mA dc, the depletion layer extends 1.5 μm.

Fig. 3 and 4 show the diode chip admittance measured, respectively at 25 and 26.4 V dc bias voltage. Each figure contains 6 heavily drawn curves corresponding to 6 different frequencies. Each of these curves represents a device line as a function of rf voltage across the chip. The curves are drawn by the X-Y recorder of the characterization system. The thin lines of equi-rf voltage are drawn in afterward. Also shown in Fig. 3 is the negative of the circuit admittance locus of the amplifier used for this diode characterization.

The following phenomenological features which indicate the transition from a conventional IMPATT mode to a high efficiency mode at large signal level can be seen from an examination of Fig. 3 and 4.

1. The magnitude of negative conductance $|G_D|$ at small signal levels decreases with frequency while it increases at large signal levels.
2. $|G_D|$ tends to remain constant, or sometimes increases with rf voltage at large signal levels after showing a rapid decrease at medium signal levels.
3. The small signal region at each frequency is distinguished from the large signal region by a characteristic bump in susceptance B_D when rf voltage increases.

Features 2 and 3 are more clearly depicted in Fig. 5, where G_D and B_D at 19 GHz are plotted as a function of rf voltage.

It is found that the diode has a maximum conversion efficiency of 26% with 2.0 W power output at 22 GHz for 26.4 V bias voltage if the series resistance of the diode is neglected.

It is believed that this transition to high efficiency mode can be attributed to the depletion width modulation as is observed in premature collection mode(2). Fig. 6 provides the graphical and qualitative explanation. Here plotted are the positions of the depletion edge and a charge packet travelling through the drift zone as a function of radial angle θ (= ωt). X_{DSS} denotes the small signal depletion edge. A half cycle sine wave, shown as a solid line, is the depletion edge for the rf voltage V_{RF2}, while a dashed curve is for the smaller voltage V_{RF1}. Three straight lines through the origin represent the paths of an electron

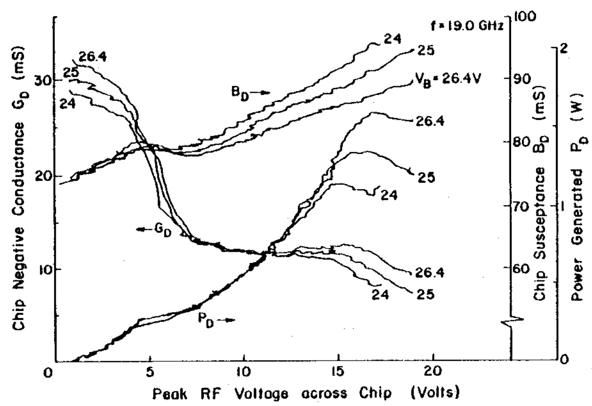

Fig. 5 Chip admittance and power generation vs. peak rf voltage across the chip.
diode: E1101 S/N2 freq: = 19.0 GHz

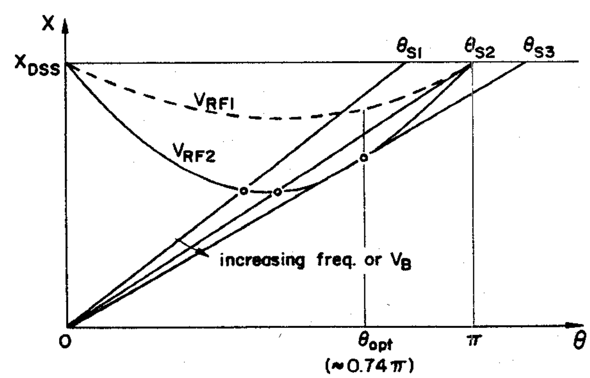

Fig. 6 Graphical explanation of high efficiency mode. Relation between depletion width modulation and charge packet collection.

charge packet at 3 different frequencies, the slopes of which give the saturated velocity. θ_s is the small signal transit angle. A circle at the intersection between a V_{RF} curve and a straight line indicates the timing at which the packet is collected.

For 25 V bias voltage the calculated small signal transit angle becomes 1.0 π at 21 GHz when the value of 5×10^6 cm/s is assumed for electron velocity. Thus the line of θ_{S2} corresponds to that for 21 GHz, θ_{S1} for lower frequency. The approximation of a pulse-like charge packet leads to the conclusion that the highest efficiency at a given rf voltage is obtained when the transit angle is 0.74 π. With these conditions kept in mind one can explain the experimental observations in Fig. 3 and 4. The effect of increased dc voltage can also be discussed by shifting the X_{DSS} line and depletion edge curves upwards in Fig. 6, or almost equivalently by decreasing the slopes of charge packet lines.

In actual diodes the transition to the high efficiency mode, as shown in Fig. 5, is somewhat obscured since the collection of a charge packet does not take place instantaneously because of the relatively large width of the packet compared to the drift zone length. This fact will set an upper limit to the frequency at which a definite transition is easily observable. A gradual transition, however, implies the possibility of designing high efficiency diodes with constant negative conductance for high power linear amplifiers.

The importance of reducing the IMPATT diode's series resistance should also be emphasized since a measured resistance of 0.3 ohms in the present diode reduces the available power output to 1.4 W with 18% efficiency at 22 GHz.

Amplifier performance

The diode has been embedded in a modified top-hat structure in Fig. 7. This circuit enables wideband operation since it provides a characteristic loop in its circuit admittance locus, as was shown in Fig. 3[3]. The loop can be reasonably tailored by changing the circuit dimensions. The typical circuit efficiency ranges from 80% to 97%, depending on frequency. Fig. 8 shows the gain vs. frequency curves of the amplifier with input power as a parameter. The bandwidth of 3.1 GHz at 3.7 ± 0.3 db gain was obtained for 1 W input power when 26.4 V dc bias voltage was applied to the diode. The solid line in Fig. 9 is the output power vs. input power of the amplifier at 20.75 GHz. The maximum output power was 3 W with 3 dB gain. The overall conversion efficiency of 22% with 1.6 W added power was observed at 21.0 GHz.

Conclusion

A high efficiency mode believed to be similar to the premature collection mode has been observed in a 20 GHz MBE GaAs IMPATT diode using a computer-aided characterization system. The diode shows an intrinsic capability of 2 W output power with 26% efficiency. However, the series resistance plays a critical role in limiting the actually available power.

Acknowledgement

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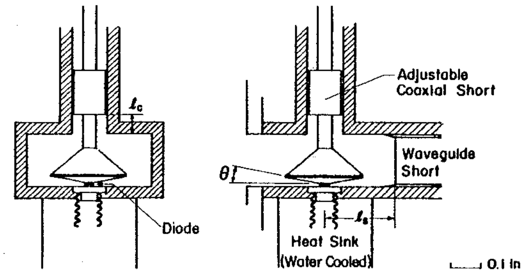

Fig. 7 Modified top-hat structure for wideband IMPATT amplifiers.

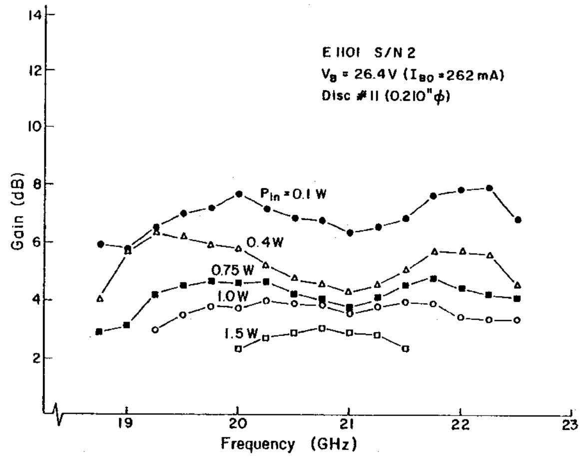

Fig. 8 Gain vs. frequency of an IMPATT amplifier.

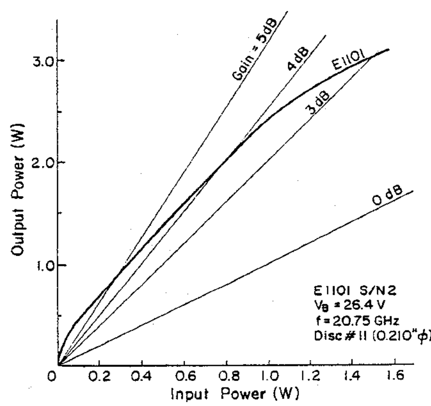

Fig. 9 Output power vs. input power of an IMPATT amplifier at 20.75 GHz.

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